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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/851,313	05/09/2001	Tatsuya Usami	NEC01P069-MSb	2820

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EXAMINER	
MALDONADO, JULIO J	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 06/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/851,313	USAMI, TATSUYA	
	Examiner	Art Unit	
	Julio J. Maldonado	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 March 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4,5,8,31,32 and 34-56* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 4, 5, 8, 31, 32 and 34-55 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yau et al. (U.S. 6,054,379) in view of Allada et al. (6,218,317 B1) alone or in combination with Chen et al. (Effects of slurry formulations on chemical-mechanical polishing of low dielectric constant polysiloxanes: hydrido-organo siloxane and methyl silsesquioxane) and the Applicants' Admitted Prior Art.

In reference to claims 1, 5, 31, 35, 39, 40, 41, 42, 46 48, 49, 52, 54 and 55, Yau et al. (Fig.10H) teach a semiconductor device having an interconnect structure including a first insulation layer (710) comprising an polymeric organic material having a dielectric constant which is lower than a silicon oxide dielectric constant; a second insulation layer (714, 716, 718) consisting of three layer and including a polysiloxane compound having an Si-H group and formed on and adhering to a top of said first insulation layer (710); a third insulation layer (722) comprising an inorganic material and formed on and adhering to a top of said second insulation layer (714), the first (710), second (714, 716, 718) and third (722) forming a multi-layered insulation film; and a plurality of wires (724) which are formed in groves formed in said multi-layered insulation film filling a space between said wires (724), wherein said second insulation layer (714, 716, 718)

comprises a hydride organosiloxane, and said second insulation layer (714, 716, 718) comprises a layer to improve an adhesion property between said first insulation layer (710) and said third insulation layer (722) (column 13, lines 12 – 663).

However, Yau et al. fail to expressly teach that said product includes a Si-H bond. However, Yau et al. teach an interconnect structure including a dielectric adhesive layer formed in a plasma reactor. This compound is the product of organosilicon compounds having the structure $SiH_a(CH_3)_b(C_2H_5)_c(C_6H_5)_d$, where a=1 to 3, b=0 to 3, c=0 to 3 and a+b+c+d=4, and oxidizing compounds such as N_2O and O_2 (Yau et al., column 4, lines 32 – 63). Yau et al. also teach using CH_3-SiH_3 as a preferred organosilicon compound. Taking this into consideration, and for purposes of providing support, Schmitt et al. to U.S. 2005/0233591 A1 teach an interconnect structure including a dielectric adhesive layer formed in a plasma reactor using reactants such as CH_3-SiH_3, and $(CH_3)_2$-SiH_2, for example, and oxidizing compounds such as N_2O and O_2, wherein said product can include CH_3-SiH_2-O- groups and $(CH_3)_2$-SiH-O- groups. (Schmitt et al., [0027] – [0033]). Since the same materials are treated the same way, the same product is obtained, and Yau et al. teach upon the claimed limitation.

Still, Yau et al. fail to disclose wherein said second insulation layer comprises methylated hydrogen silsesquioxane film (MHSQ) at a thickness of about 50 nm, wherein said dielectric layer includes repeating units of $(SiCH_3O_2)_n$, $(SiO_2H)_n$ and $(SiO_3)_n$, wherein a molar ratio of $(SiO_2H)_n$ to a total of said repeating units is at least 0.2. However, Allada et al. (Figs.1a-1b) in a related art to the formation of copper

interconnect structures teach a second insulating film comprising a methylated hydrido organo siloxane polymer (HOSP), wherein said polymer can be formed by spin coating processes or by conventional CVD processes (column 2, lines 7 – 67).

Furthermore, according to Chen (Fig.1), methylated hydrido organo siloxane polymer (HOSP) includes repeating units of $(SiCH_3O_2)_n$, $(SiO_2H)_n$ and $(SiO_3)_n$, wherein a molar ratio of $(SiO_2H)_n$ to a total of said repeating units is at least 0.2.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to use the insulating layer as taught by Allada et al. in the interconnect formation structure of Yau et al., since this dielectric layers exhibit low dielectric constants and also have better adhesion properties than conventional dielectric layers (Allada et al., column 1, lines 37 – 60 and column 2, lines 36-48).

The combined teachings of Yau et al. and Allada et al. fail to teach wherein said MHSQ film comprises a thickness of about 50 nm. Notwithstanding, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose these particular dimensions because applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531 F.2d 1048, 189 USPQ

143 (CCPA 1976); Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

The combination of Yau et al., Allada et al. and Chen et al. teach wherein the first insulating layer is selected from a group including parylene, FSG, silicon oxide, or the like (Yau et al., column 13, lines 12 – 16) and wherein metal lines can be included on the substrate wherein said first dielectric layer covers a space between said metal lines (Yau et al., column 10, line 18 – column 11, line 43), but fail to teach wherein the first insulation layer is an organopolysiloxane including methyl silsesquioxane (MSQ) and wherein said wires connect a plurality of gate electrodes formed on said substrate with an upper level in the device, said first insulation layer formed on and between said gate electrodes, wherein said plurality of wires comprises a contact which contacts a diffusion region formed in said substrate between said plurality of gate regions, wherein a spaced formed between adjacent gate electrodes in said plurality of gate electrodes is filled with said first insulation layer and wherein a spaced formed between adjacent gate electrodes in said plurality of gate electrodes filled with said first insulation layer. However, the prior art (Instant Figs.8a-9b) teaches a device having a plurality of gate electrodes (60) having diffusion regions (54) formed on a substrate (51); and a first insulation layer (55) over said substrate (51) having a wiring connection between the gate electrodes through a diffusion region (54) locates between said gate electrodes (60), wherein said first insulation layer includes methyl silsesquioxane, and wherein said

wiring connects said gate electrodes to an upper level (Instant page 2, lines 5 – 8 and page 5, lines 9 – 24).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Yau et al., Allada et al. and Chen et al. with the teachings of the prior art to substitute the dielectric material taught by Yau et al. for the SOG material disclosed by the prior art because using MSQ reduces crosstalk between metal wires (Instant page 2, lines 12 – 15) and because the selection of a known material based on its suitability for its intended use supported a prima facie obviousness. MPEP 2144.07. It would also have been obvious to one of ordinary skill in the art to combine the teachings of Yau et al., Allada et al., Chen et al. and the prior art to substitute the metal lines of Yau et al., Allada et al., Chen et al. with the electrodes disclosed in the prior art to arrive at the claimed invention.

In reference to claims 4 and 8, the combined teachings of Yau et al., Allada et al., Chen et al. and the prior art teach wherein said third insulation layer comprises at least one material selected from the group including silicon oxide (column 13, lines 19 – 22).

In reference to claims 34 and 47, the combined teachings of Yau et al., Allada et al., Chen et al. and the prior art teach wherein said first insulation layer comprises a thickness greater than a thickness of said second insulation layer; and wherein said first insulation layer can have a thickness greater than a thickness of said third insulation layer (Yau et al., column 13, lines 12 – 22).

In reference to claim 37, the combined teachings of Yau et al., Allada et al., Chen et al. and the prior art teach wherein a bottom of said groove is formed on a same surface as said first insulation layer (Yau et al., Fig.10H).

In reference to claim 38, the combined teachings of Yau et al., Allada et al., Chen et al. and the prior art teach wherein said plurality of wires comprises copper wires (Yau et al., column 13, lines 47 – 63).

In reference to claim 43, the combined teachings of Yau et al., Allada et al., Chen et al. and the prior art teach wherein said first insulation layer, said second insulation layer and said third insulation layer of said multi-layered insulation film comprise substantially uniform widths (Yau et al., Fig.10H).

In reference to claim 44, the combined teachings of Yau et al., Allada et al., Chen et al. and the prior art teach wherein a surface of said multi-layered film is substantially coplanar with a surface of said plurality of wires (Yau et al., Fig.10H).

In reference to claim 45, the combined teachings of Yau et al., Allada et al., Chen et al. and the prior art teach wherein said second insulation layer is formed by plasma CVD (Yau et al., column 4, line 19 – column 5, line 19).

In reference to claim 53, the combined teachings of Yau et al., Allada et al., Chen et al. and the prior art teach a silicon nitride layer, said first insulation layer being formed in said silicon nitride layer and said plurality of grooves having a bottom defied by an upper surface of said silicon nitride layer (Allada et al., column 2, lines 7 – 57).

3. Claim 56 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yau et al. (U.S. 6,054,379) in view of Allada et al. (6,218,317 B1) alone or in combination with

Chen et al. (Effects of slurry formulations on chemical-mechanical polishing of low dielectric constant polysiloxanes: hydrido-organo siloxane and methyl silsesquioxane) and the Applicants' Admitted Prior Art as applied to claims 1, 4, 5, 8, 31, 32 and 34-55 above, and further in view of Lu et al. (U.S. 6,008,540).

The combined teachings of Yau et al., Allada et al., Chen and the prior art substantially teach a substrate including metal lines (Yau et al., Fig.6A), but fail to teach a substrate having a plurality of gate electrodes formed on said semiconductor substrate; and a plurality of impurity diffusion regions formed in the semiconductor substrate, wherein said first, second and third insulation layers are formed on said plurality of gate electrodes, and wherein said plurality of grooves comprises a plurality of impurity diffusion regions and between said plurality of gate electrodes. However, Lu et al. (Figs.1-3) teach an interconnect structure formed in a dielectric stack (342, 344, 346), wherein said dielectric stack further includes an adhesion layer (344) and wherein said interconnect structure further includes a plurality of gate electrodes (112) formed on said semiconductor substrate (102); and a plurality of impurity diffusion regions (114) formed in the semiconductor substrate (102), wherein dielectric stack (342, 344, 346) are formed on said plurality of gate electrodes (112), and wherein a plurality of grooves comprises a plurality of contact holes formed in said dielectric stack (342, 344, 346) on said plurality of impurity diffusion regions (114) and between said plurality of gate electrodes (342, 344, 346) (Lu et al., column 5, line 50 – column 6, line 67). It would have been within the scope of one of ordinary skill in the art to combine the teachings of Yau et al., Allada et al., Chen and the prior art and Lu et al. to enable the substrate of

Yau et al., Allada et al., Chen and the prior art to include the devices according to the teachings of Lu et al. because one of ordinary skill in the art at the time the invention was made would have been motivated to look to materials included in the substrate of Yau et al., Allada et al., Chen and the prior art and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

Response to Arguments

4. Applicant's arguments filed 3/28/2006 have been fully considered but they are not persuasive.

In response to Applicants arguments, the layers are adhered because they hold fast, or stick by or as if by gluing, suction, grasping and fusing.

Applicants argue, "...Applicants submits that [the prior art of record] does not teach or suggest "wherein said second insulation layer comprises a methylated hydrogen silsesquioxane (MHSQ) layer which adheres to said organosiloxane film and said inorganic material", as recited in claim 1...the improved adhesion may help to allow a surface of the third insulation layer to be planarized together with a surface of a wire formed in one of the grooves without causing peeling of the third insulation layer...". In response to this argument, the above mentioned advantages are ambiguous because it "may help to allow a surface of the third insulation layer to be planarized..." as argued. Therefore, there could be or could not be an advantage of combining these two layers.

Furthermore, the layers are adhered because they hold fast or stick by or as if by gluing, suction, grasping, or fusing.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

6. Applicants are encouraged, where appropriate, to check Patent Application Information Retrieval (PAIR) (http://portal.uspto.gov/external/portal/pair) which provides applicants direct secure access to their own patent application status information, as well as to general patent information publicly available.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Julio J. Maldonado whose telephone number is (571) 272-1864. The examiner can normally be reached on Monday through Friday.

8. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith, can be reached on (571) 272-1907. The fax number for this

group is 571-273-8300. Updates can be found at

http://www.uspto.gov/web/info/2800.htm.

Julio J. Maldonado
Patent Examiner
Art Unit 2823

Julio J. Maldonado
June 1, 2006

GEORGE R. FOURSON
PRIMARY EXAMINER